Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A semiconductor package manufactured by a method of manufacturing a semiconductor package containing a capacitor portion, the method comprising the steps of:
forming a first wiring layer on an insulative base member, the first wiring layer being patterned in a predetermined shape for serving as a first electrode layer of the capacitor portion;
forming a resin layer on a surface of the first wiring layer for serving as a dielectric layer of the capacitor layer by an electrophoretic deposition process;
forming a second wiring layer on the insulative base member inclusive of the resin layer, the second wiring layer being patterned in a predetermined shape for serving as a second electrode layer of the capacitor portion;
forming a laminated core portion by preparing a predetermined number of printed wiring boards each of which is a structure made by forming the first wiring layer, the resin layer and the second wiring layer sequentially on the insulative base member, and by laminating the respective printed wiring boards by thermal press in a vacuum ambiance while interposing prepregs severally between the printed wiring boards;

forming through holes on the laminated core portion severally in a region where the resin layer is formed via the first wiring layer on the insulative base member but uncovered with the second wiring layer, and in a region where the second wiring layer is formed directly on the insulative base member;

filling insides of the through holes with conductors;

forming third wiring layers patterned into predetermined shapes on both surfaces of the laminated core portion inclusive of the through holes filled with the conductors;

forming insulating layers on both surfaces of the laminated core portion inclusive of the third wiring layers;

forming via holes in predetermined positions of the insulating layer so as to reach respective pads of the third wiring layer;

forming a multilayer wiring board by sequentially repeating formation of a patterned wiring layer, an insulating layer and via holes so as to constitute a required number of layers, and finally by filling insides of the via holes with conductors;

forming protective films on both surfaces of the multilayer wiring board and then forming openings in the respective protective films at portions corresponding to positions of the conductors inside the via holes; and

bonding external connection terminals to the conductors exposed from the openings formed in one of the protec-

tive films.

[c2] 2. A semiconductor device comprising:
the semiconductor package according to claim 1; and
a semiconductor element mounted on an opposite side of the semiconductor package to the side where the external connection terminals are bonded, electrode terminals of the semiconductor element being electrically connected to the conductors exposed from the openings formed in the protective film.

[c3] 3. A semiconductor package manufactured by a method of manufacturing a semiconductor package containing a capacitor portion, the method comprising the steps of:
forming a first wiring layer on an insulative base member, the first wiring layer being patterned in a predetermined shape for serving as a first electrode layer of the capacitor portion;
forming a resin layer on a surface of the first wiring layer for serving as a dielectric layer of the capacitor layer by an electrophoretic deposition process;
forming a second wiring layer on the insulative base member inclusive of the resin layer, the second wiring layer being patterned in a predetermined shape for serving as a second electrode layer of the capacitor portion;
forming a laminated core portion by preparing a predetermined number of printed wiring boards each of which

is a structure made by forming the first wiring layer, the resin layer and the second wiring layer sequentially on the insulative base member, and by laminating the respective printed wiring boards by thermal press in a vacuum ambiance while interposing prepregs severally between the printed wiring boards;

forming through holes on the laminated core portion severally in a region where the resin layer is formed via the first wiring layer on the insulative base member but uncovered with the second wiring layer, and in a region where the second wiring layer is formed directly on the insulative base member;

filling insides of the through holes with conductors;

forming third wiring layers patterned into predetermined shapes on both surfaces of the laminated core portion inclusive of the through holes filled with the conductors;

forming insulating layers on both surfaces of the laminated core portion inclusive of the third wiring layers;

forming via holes in predetermined positions of the insulating layer so as to reach respective pads of the third wiring layer;

forming a multilayer wiring board by sequentially repeating formation of a patterned wiring layer, an insulating layer and via holes so as to constitute a required number of layers, and finally by filling insides of the via holes with conductors;

forming protective films on both surfaces of the multi-layer wiring board and then forming openings in the respective protective films at portions corresponding to positions of the conductors inside the via holes;
forming plated films on the conductors exposed from the openings of the respective protective films; and
bonding external connection terminals to the conductors exposed from the openings formed in one of the protective films.

[c4] 4. A semiconductor device comprising:
the semiconductor package according to claim 3; and
a semiconductor element mounted on an opposite side of the semiconductor package to the side where the external connection terminals are bonded, electrode terminals of the semiconductor element being electrically connected to the conductors exposed from the openings formed in the protective film.